SEMICONDUCTOR PACKAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims priority under 35 U.S.C 119(a) to Korean Application Nos. 10-2015-0027589 and 10-2015-0084339 filed on Feb. 26, 2015 and Jun. 15, 2015, respectively, in the Korean intellectual property Office, which are incorporated herein by references in their entirety.

BACKGROUND

1. Technical Field

Various embodiments of the present disclosure generally relate to a packaging technology, and more particularly to semiconductor devices including an elastic buffer layer and a trench.

2. Related Art

With broadening uses of compact, portable electronic systems, semiconductor devices continue to shrink in size. Moreover, demands for high-performance electronic systems have led to many advances in multi-functional semiconductor devices. Recent developments in wearable electronic systems are leading to demands for bendable and flexible semiconductor packages.

A semiconductor package includes a substrate, semiconductor chips mounted on the substrate, an interconnection member for connecting the semiconductor chips to conductive lines on the substrate. It is possible to reduce the thickness of the substrate or semiconductor chips disposed on the substrate so that the semiconductor package can be bent. However, it is difficult for the interconnection member to be bent without damaging its functionality. Tensile stress or compressive stress, which can be applied when the interconnection member is warped or twisted, may cause the interconnection member to be separated from a connection pad or to be broken, and thereby causes the semiconductor package to malfunction. Accordingly, bendable and flexible semiconductor packages require a package structure capable of maintaining the electrical connections between the interconnection members and the semiconductor chips/substrate even when the semiconductor package is warped or twisted.

SUMMARY

According to an embodiment, there is provided a semiconductor device. The semiconductor device includes a substrate, an elastic buffer layer disposed on a surface of the substrate, wiring patterns disposed on a surface of the elastic buffer layer, and a semiconductor chip disposed on another surface of the elastic buffer layer opposite to the substrate. The semiconductor chip includes trenches disposed therein. Interconnection members are disposed to electrically connect the wiring patterns to the substrate. Each of the interconnection members has one end electrically connected to one of the wiring patterns and the other end electrically connected to the substrate.

The elastic buffer layer includes an insulation material having a Young's modulus of about 0.01 GPa to about 0.1 GPa. The insulation material includes one or more of silicone resin and silicone rubber. The semiconductor chip includes a plurality of trenches spaced apart from each other and facing the elastic buffer layer. The trenches have a predetermined depth from a surface of the semiconductor chip facing the elastic buffer layer. The trenches are covered with the elastic buffer layer to provide a cavity. Each of the wiring patterns includes a first portion disposed to overlap with one of the trenches, a couple of second portions extending from both ends of the first portion in two opposite directions and having a curved line shape, and a couple of third portions extending from the second portions in an opposite direction to the first portion and having a straight line shape. Each of the second portions has a sine wave shape. The first portion is a landing pad connected to one of the interconnection members. The interconnection members are disposed to overlap with the trenches, respectively. Each of the interconnection members includes a pillar portion, and a protrusion portion extending from an end of the pillar portion to have a hemispherical shape, wherein the protrusion portion is connected to one of the wiring patterns. Each of the interconnection members includes copper. The semiconductor chip and the elastic buffer layer are covered with a molding member. A space between the elastic buffer layer and the substrate is filled with a flexible molding member. The flexible molding member includes one or more of silicone resin and silicone rubber.

According to another embodiment, there is provided a semiconductor device. The semiconductor device includes a semiconductor chip having a first surface and a second surface opposite to the first surface, a substrate disposed on the first surface of the semiconductor chip, and an insulation layer disposed between the semiconductor chip and the substrate. The insulation layer includes trenches disposed therein, and the trenches have a predetermined depth. An elastic buffer layer is disposed between the insulation layer and the substrate. Lower wiring patterns are disposed in the elastic buffer layer. Each of the lower wiring patterns includes a landing pad aligned with any one of the trenches. Interconnection members are disposed to electrically connect the landing pads to the substrate. Each of the interconnection members has one end electrically connected to one of the landing pads and the other end electrically connected to the substrate.

According to another embodiment, there is provided a semiconductor device. The semiconductor device includes a first substrate and a second substrate. The second substrate is disposed over the first substrate, and the second substrate includes a first surface and a second surface opposite to the first surface. A trench is disposed in the second substrate to be adjacent to the second surface. An elastic buffer layer is disposed on the second surface of the second substrate, and the elastic buffer layer has an opening disposed on its surface facing the first substrate. A lower wiring pattern is disposed inside the elastic buffer layer, and the lower wiring pattern includes a landing pad disposed to be aligned to the trench. An interconnection member is disposed to electrically connect the first substrate to the second substrate. One end of the interconnection member is connected to the lower wiring pattern, and the other end is connected to the first substrate.

The second substrate further includes an outer circuit wiring pattern disposed on the first surface and a via electrode penetrating the second substrate from the first surface to the second surface, wherein one of both ends of the via electrode is connected to the outer circuit wiring pattern and the other end is connected to the lower wiring pattern. The elastic buffer layer is disposed to cover the opened portion of the upper portion of the trench on the second surface of the second substrate, and wherein the landing pad is disposed on the elastic buffer layer. The trench is disposed to have a predetermined depth from the second surface of the second substrate, and the elastic buffer layer is disposed to cover the opened portion of the upper portion of the trench, and a cavity is disposed between the trench and